REMARKS

Claims 1-21 are all the claims pending in the application. Claims 1-21 stand rejected on prior art grounds. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Aguilar, et al. (U.S. Pat. No. 6,199,137) in view of Garland, et al. 6,389,120. Applicants respectfully traverse these rejections because the prior art of record does not teach or suggest selectively engaging different numbers of serial lanes to alter the speed of data passing through a core. The Office Action admits that Aguilar does not disclose selectively engaging serial lanes to alter speed of data passing through the core. The Office Action refers to Garland as teaching such a feature.

Most succinctly, the Office Action argues, in paragraph 12 on page 6, that the router/multiplexer 202 and the server 106 containing the buffer 120 could be considered the core and that the multiplexer 202 and buffer 120 would perform a function of adjusting to different data rates. However, the claim language requires that the selector (multiplexer) selectively engage different numbers of serial lanes so as to alter the speed of data passing through the core. To the contrary, Garland always utilizes the same number of serial lanes and the same number of buffers and does not increase or decrease the number of serial lanes or buffers engaged so as to alter the speed of data passing through the core. In Garland, the router/multiplexer 202 only selects between data lines 208 serving a first server 204 and data lines 208 serving a second server 204. The data lines 210 between the multiplexer 202 and the server/buffer 106/120 are continuous in Garland indicating that the same number of data lines 210 are always used and indicating that the same number of buffers 120 are similarly always used. In other words, the multiplexer 202 only selects between the data lines 208 and does not select between the data

lines 210. Therefore, Garland does not perform any selection among the data lines 210, but instead only selects between one set of data lines 208 and another set of data lines 208 serving the different servers 204, 206 to allow the server termination switch 106 to communicate with either the first server 204 or the second server 206. Because the multiplexer 202 does not select from among the data lines 210, Garland cannot selectively engage a greater or smaller number of serial lanes (each of which includes at least one buffer, as defined by depending claims 3, 10, and 17). This is true even if only a subset of data lines 210 are utilized depending upon which server 204, 206 is selected by the multiplexer 202, because the same number of data lines 210 will always be utilized and the same number of buffers 120 will also always be utilized.

Therefore, it is Applicants' position that Garland does not teach or suggest the claimed operation where the selector "selectively engages different numbers of said serial lanes to alter a speed of data passing through said core" as defined by independent claims 1, 8, and 15. As shown in Applicants' Figure 2B, the multiplexers 215, 236 selectively engage a different number of data lanes 225 (e.g., alter the lane width) in order to perform a speed reduction between the transmission media 280 and the ASIC 246. For example, with the exemplary structure shown in FIG. 2B, the invention can perform speed reduction by simultaneously transmitting the data along four lanes.

To illustrate the utility of the invention, given that 12 data lanes are used in a network, when in a 4X reduction mode of operation, physical data lanes 4-11 can be used as wider extensions of lanes 0-3. Further, when in a 1X mode of operation using these 12 data lanes, FIFOs for data lanes 1-11 can be a wider extension of the FIFO used for data lane 0, thereby achieving up to a 12X speed reduction. Thus, when data is accessed at the transmission media 280, by using the multiplexers 215, 236, the upper link layer 250 can access wider data at a slower rate. The invention also produces an advantage in that receive elastic FIFO buffers 220 perform the function of the frequency correction portion 260 and correct any frequency deviations which may occur along the transmission media 280. FIFO buffers 220, 230 also modify the frequency of the signal to that desired by the ASIC 246. Therefore, the FIFO buffers 220 perform the functions that were previously performed by FIFO buffers 251 and 261 shown in

FIG. 2A, thereby reducing the number of buffers within the core logic 210. This decrease in the number of buffers within the core logic 210 reduces power consumption, increases processing speed and decreases the chip area consumed by the core logic 210.

Thus, as mentioned above, Aguilar does not teach selectively engaging serial lanes to alter the data speed and Garland also does not teach this feature. Therefore, the proposed combination of Aguilar and Garland does not teach or suggest the claimed operation where the selector "selectively engages different numbers of said serial lanes to alter a speed of data passing through said core" as defined by independent claims 1, 8, and 15. Therefore, it is Applicants' position that the proposed combination of Aguilar and Garland does not render obvious independent claims 1, 8, and 15 and that such claims are patentable over the prior art of record. Further, dependent claims 2-7, 9-14, and 16-21 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-21, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

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Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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